

z17 Channel Performance Analysis From The New Guy

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35 YEARS
OF PERFORMANCE
MANAGEMENT

Uh oh, there's I/O problems...

Introduction

- **What is a Channel?**

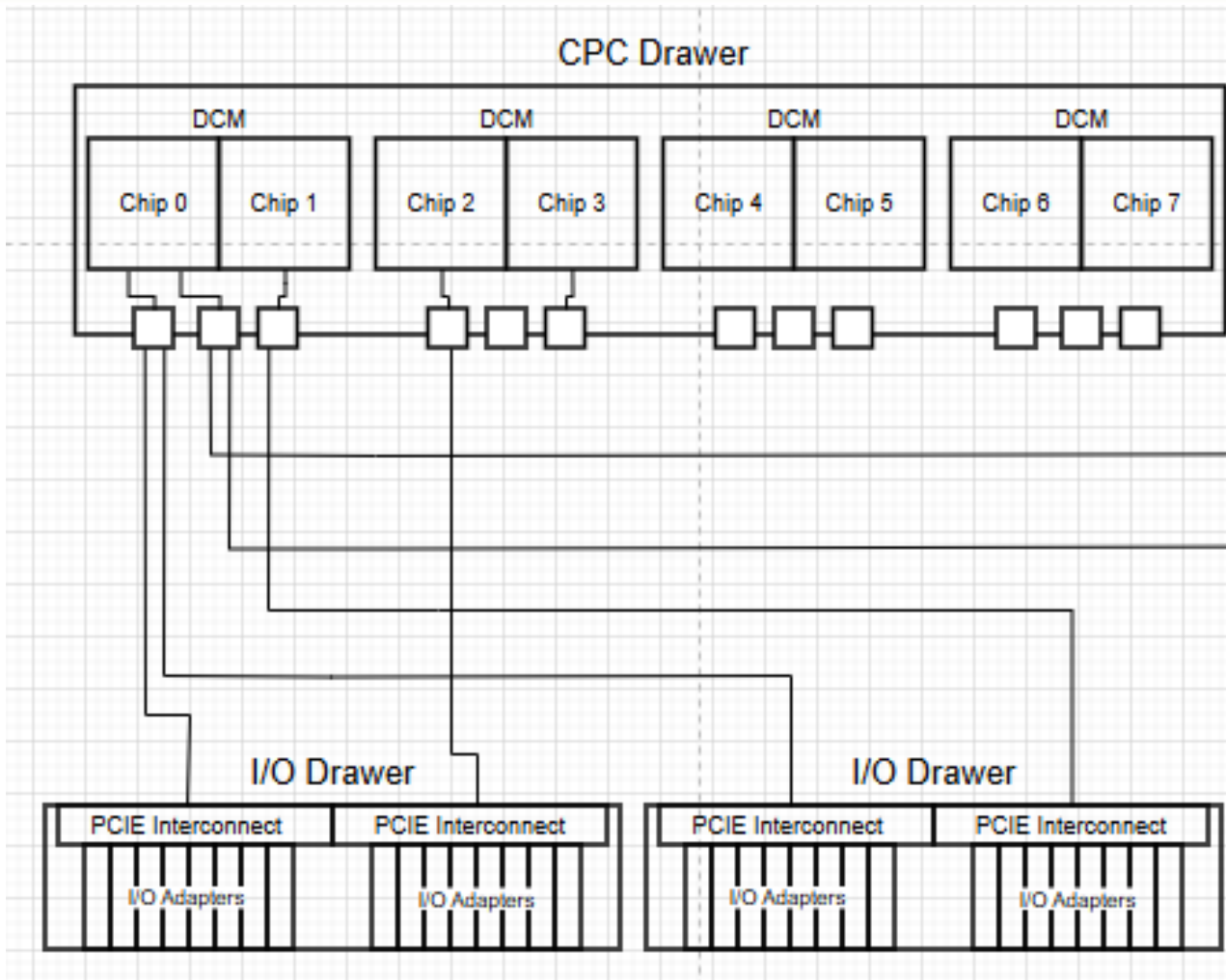
z17 Channel Architecture Changes

- **Network Express Adapter**
- **FICON Express32-4P Adapter**
- **Data Processing Unit (DPU)**

z17 Channel Performance Analysis

- **Basis of Channel Performance Analysis**
- **z17 Channel Components/Metrics**

What is a Channel?



Sample z16 drawer configuration

- **Channel** - a single I/O interface between a channel subsystem (on chip) and one or more control units
- **Channel Architecture** - Structure, behavior and components related to channels

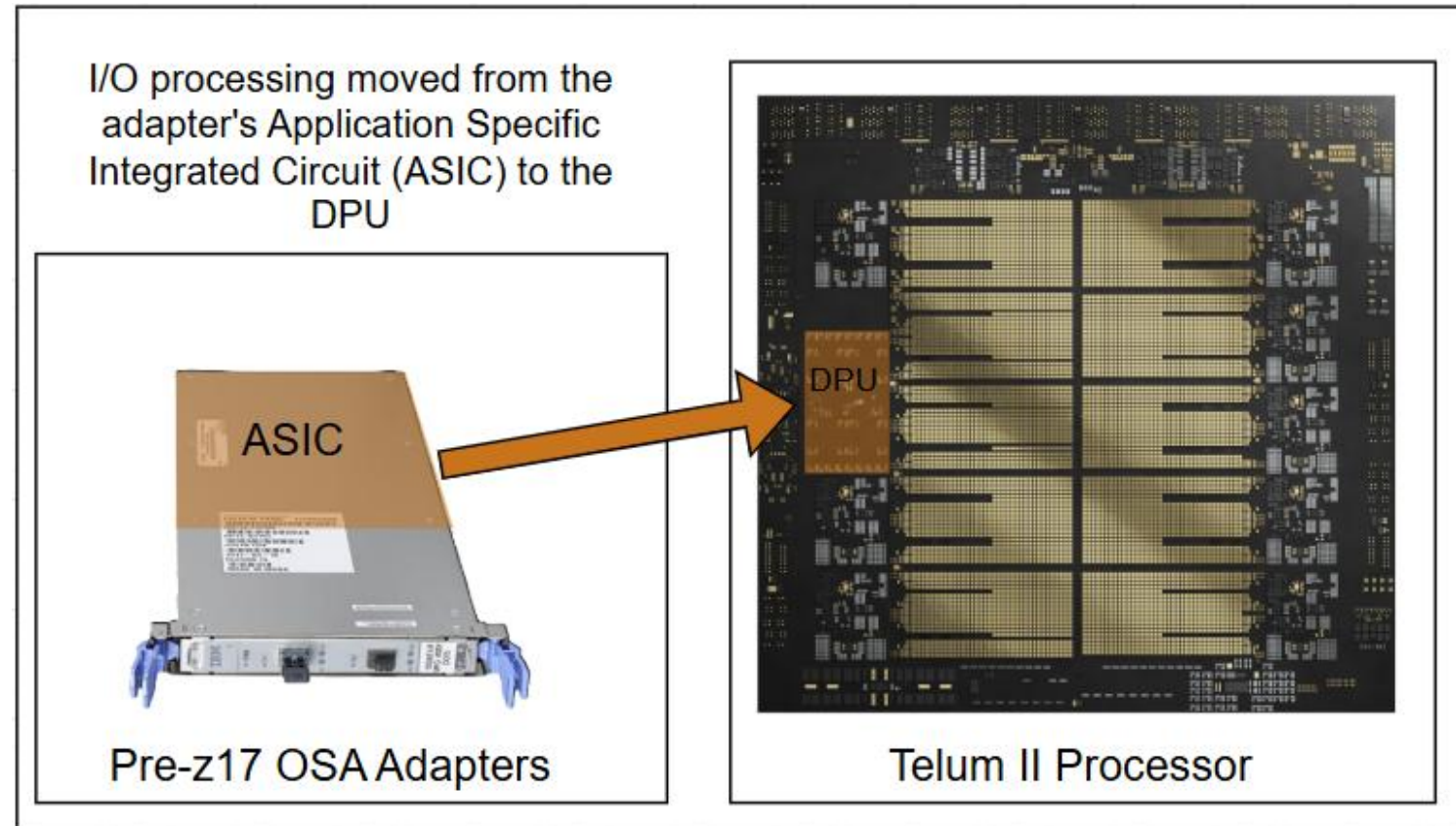
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z17 Channel Architecture Changes

Network Express Adapter

Overview

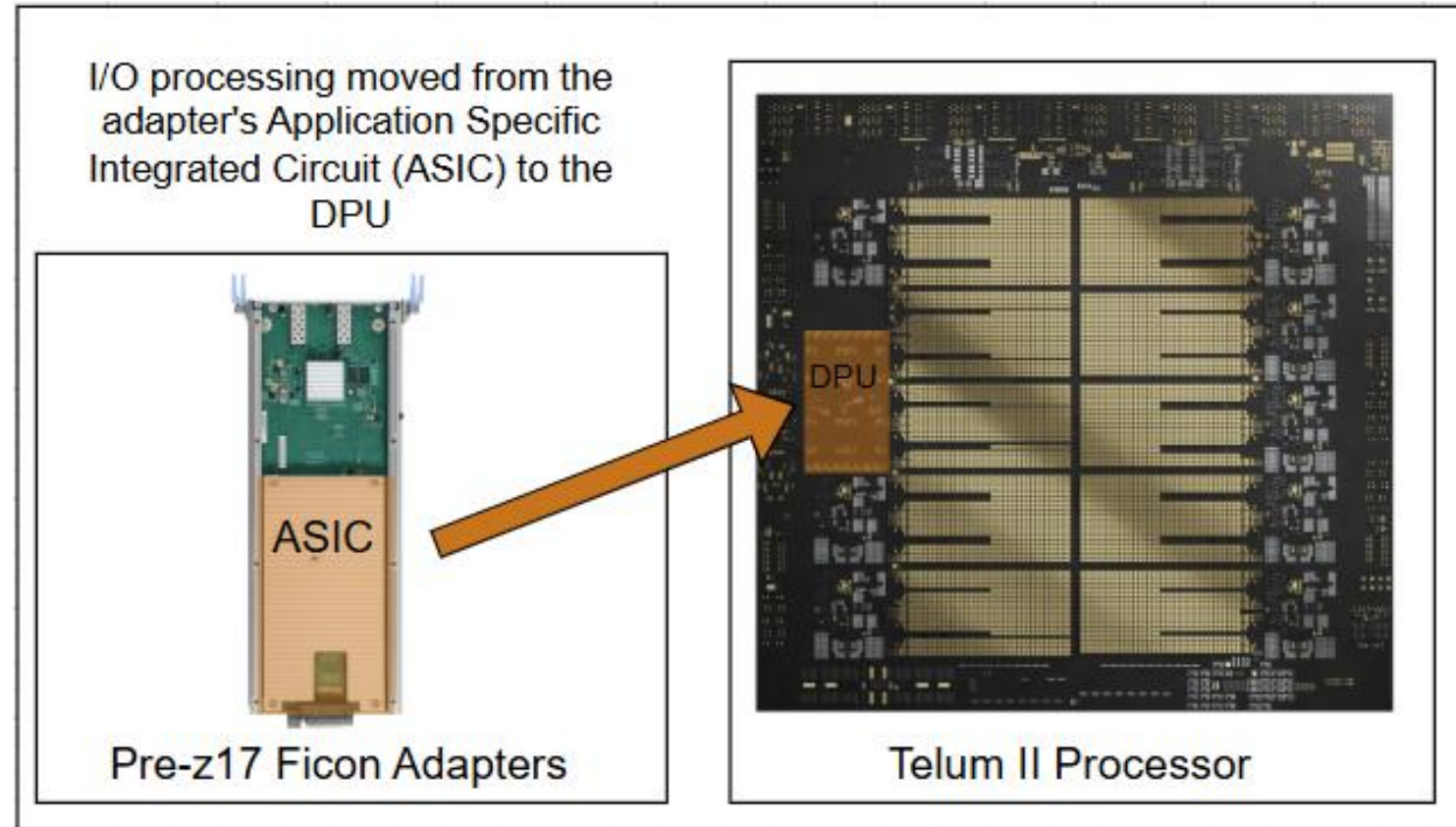
- Same functionality as older OSA and RoCE adapters
- ASICs removed
- I/O Processing is performed on the Data Processing Unit (DPU) rather than the ASIC



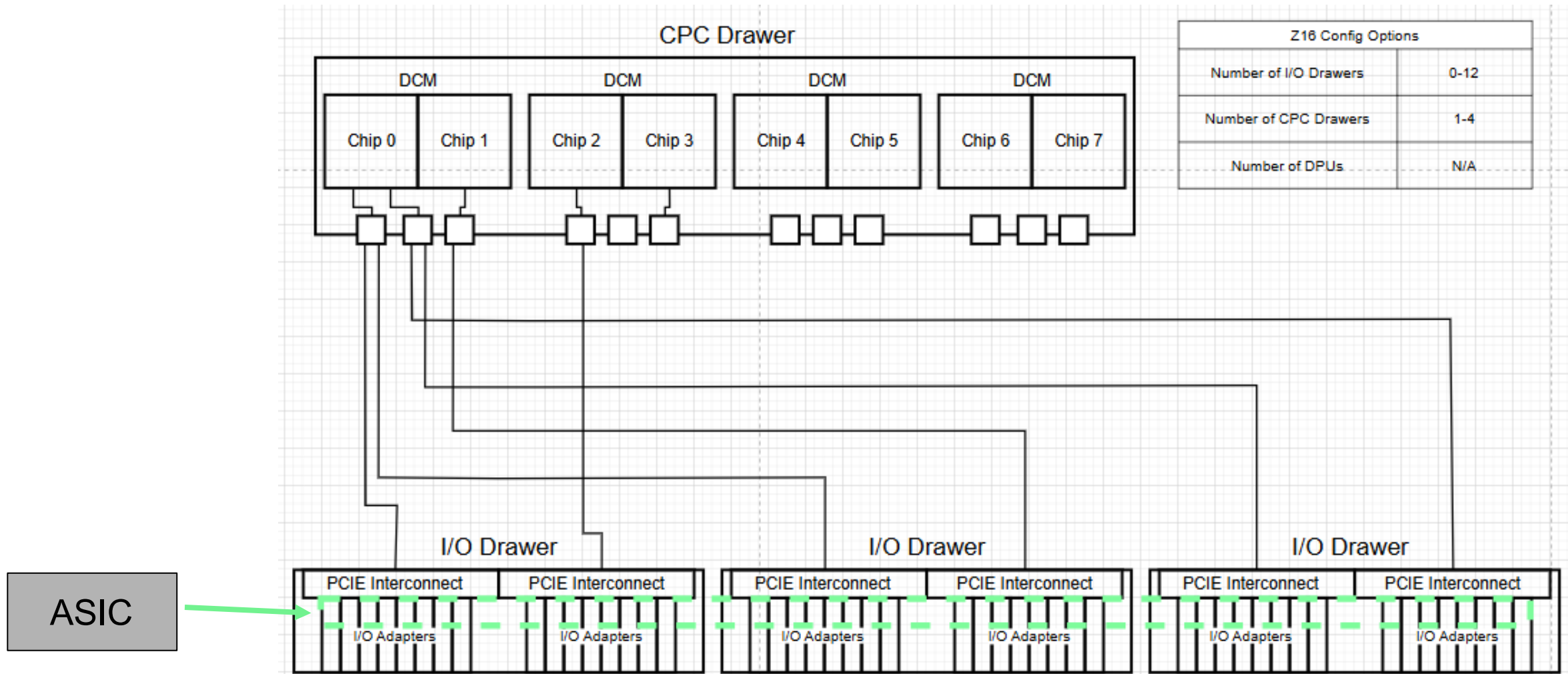
FICON Express 32-4P Adapter

Overview

- Same Functionality as older FICON adapters
- ASICs removed
- I/O Processing is performed on the DPU rather than the ASIC

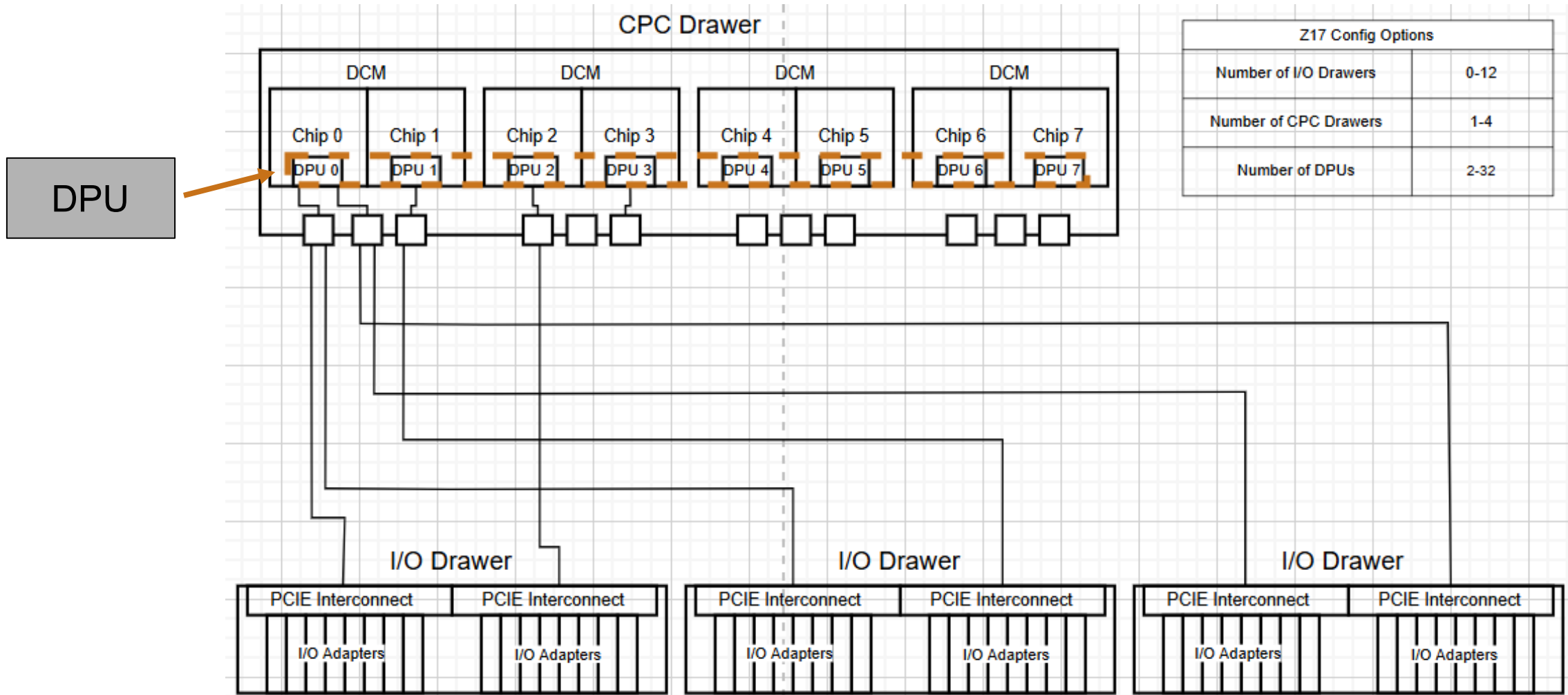


Pre-z17 I/O Processing



Sample z16 I/O drawer Configuration

Post-z17 I/O Processing



Z17 Config Options	
Number of I/O Drawers	0-12
Number of CPC Drawers	1-4
Number of DPUs	2-32

Sample z17 I/O drawer Configuration

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z17 Channel Performance Analysis

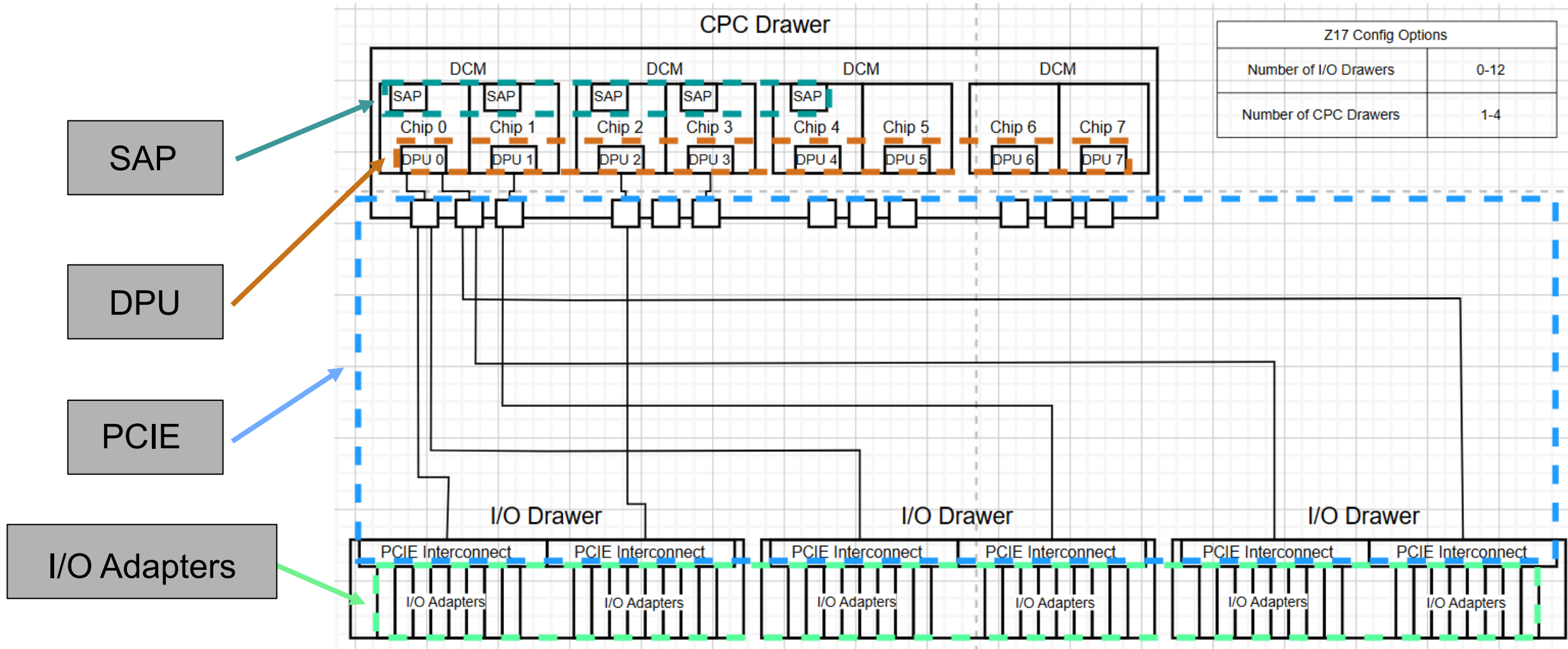
Basis of Channel Performance Analysis

- Channels are made of up of a pipeline of components
- Data can only travel as fast as the slowest component
- Channel performance analysis is based of understanding each of these components and finding which components are/will be overutilized



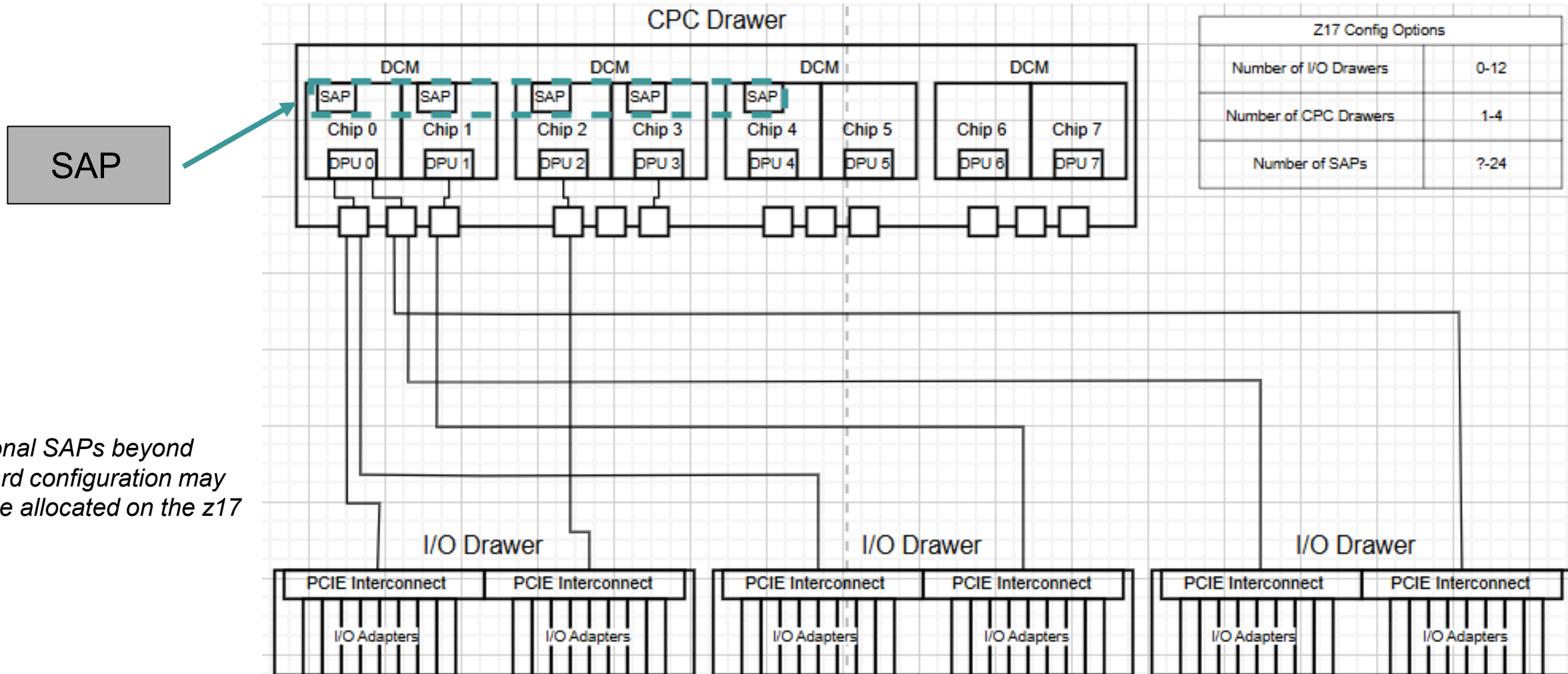
Roads much like channels are only as fast as their slowest component. The above road only has as much “car throughput” as a 2 lane road even though most of it is 3 lanes wide

z17 Channel Components



Sample z17 I/O drawer Configuration

z17 Channel Components - SAP



*Note:
Additional SAPs beyond
standard configuration may
NOT be allocated on the z17*

Sample z17 I/O drawer Configuration

z17 Channel Components – SAP

Description

- I/O processing unit configured to manage I/O operations

Relevant Performance Details

- SAPs are not utilized by
 - OSAs
 - Network Express Adapters
 - FCP channels
- SAPs share the total workload amongst themselves

Notes:

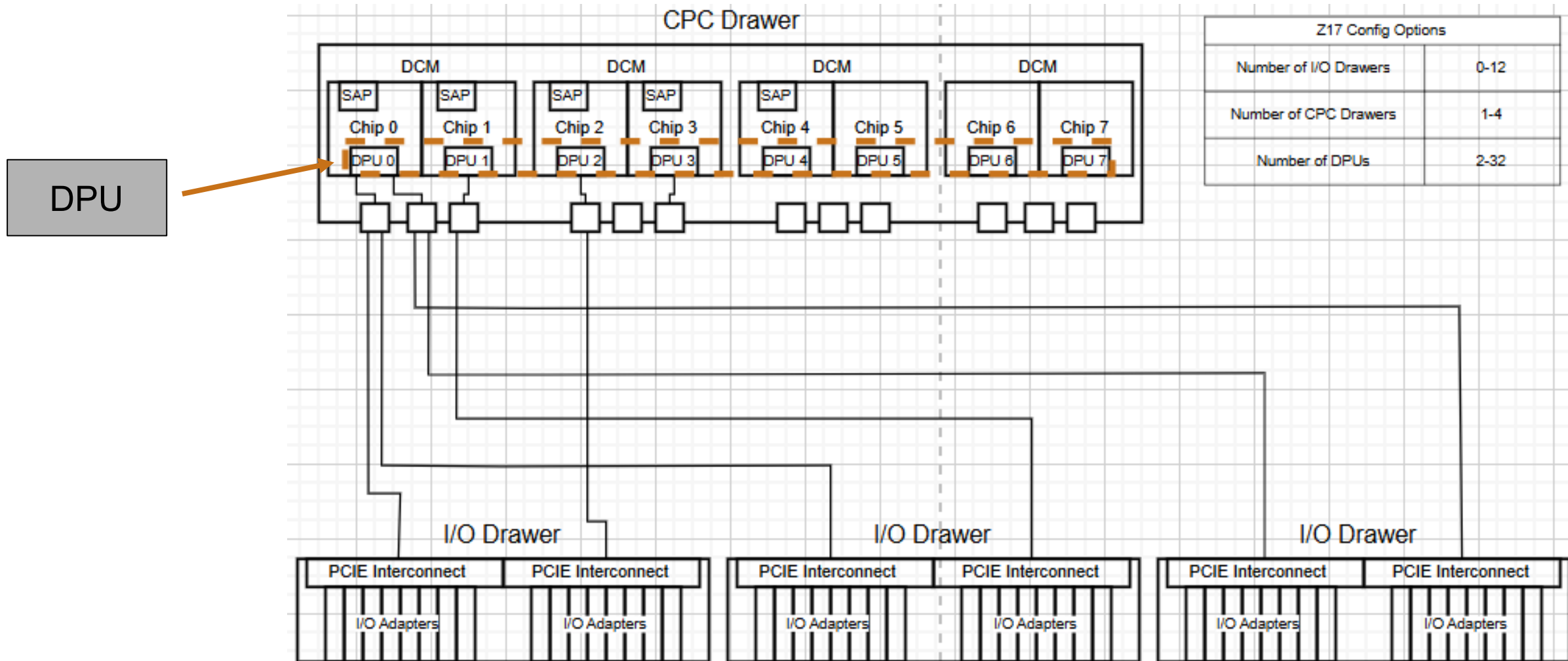
Each SAP is represented by 2 I/O threads as a result of SMT

SAP – System Assist Processor

I/O Proc Nbr	<Pct Busy>	<Pct Util>	<Rate/Second>	<I/O Processor>	<Percent of Strts busy-->	<chan switch>	<CtlUnit>	<Device>
0	1.9	98.1	1749	4718	0.1	0	0	0
1	0.7	99.3	1749	28	0.0	0	0	0
2	36.8	63.2	1748	5406	0.0	0	0	0
3	1.0	99.0	1747	46	0.0	0	0	0
4	7.8	92.2	1748	3134	0.0	0	0	0
5	0.9	99.1	1748	27	0.0	0	0	0
6	32.6	67.4	1749	2034	0.0	0	0	0
7	3.9	96.1	1749	77	0.0	0	0	0
8	7.0	93.0	1748	3354	0.0	0	0	0
9	3.5	96.5	1747	109	0.0	0	0	0
10	1.4	98.6	1747	3388	0.1	0	0	0
11	2.2	97.8	1748	120	0.0	0	0	0
12	2.5	97.5	1749	5656	0.1	0	0	0
13	3.4	96.6	1748	27	0.0	0	0	0
14	6.6	93.4	1748	4217	0.0	0	0	0
15	1.4	98.6	1748	24	0.0	0	0	0
16	1.6	98.4	1748	3337	0.1	0	0	0
17	1.4	98.6	1748	23	0.0	0	0	0
18	7.1	92.9	1748	3373	0.0	0	0	0
19	1.3	98.7	1748	24	0.0	0	0	0
20	1.6	98.4	1748	3298	0.0	0	0	0
21	1.3	98.7	1749	11	0.0	0	0	0
22	1.2	98.8	1749	1955	0.0	0	0	0
23	0.6	99.4	1749	6	0.0	0	0	0
24	2.1	97.9	1749	4754	0.1	0	0	0

Report displaying I/O Processor Metrics by Processor Number

z17 Channel Components - DPU



Sample z17 I/O drawer Configuration

z17 Channel Components - DPU

Description

- I/O processor responsible for packet construction, inspection and routing

Relevant Performance Details

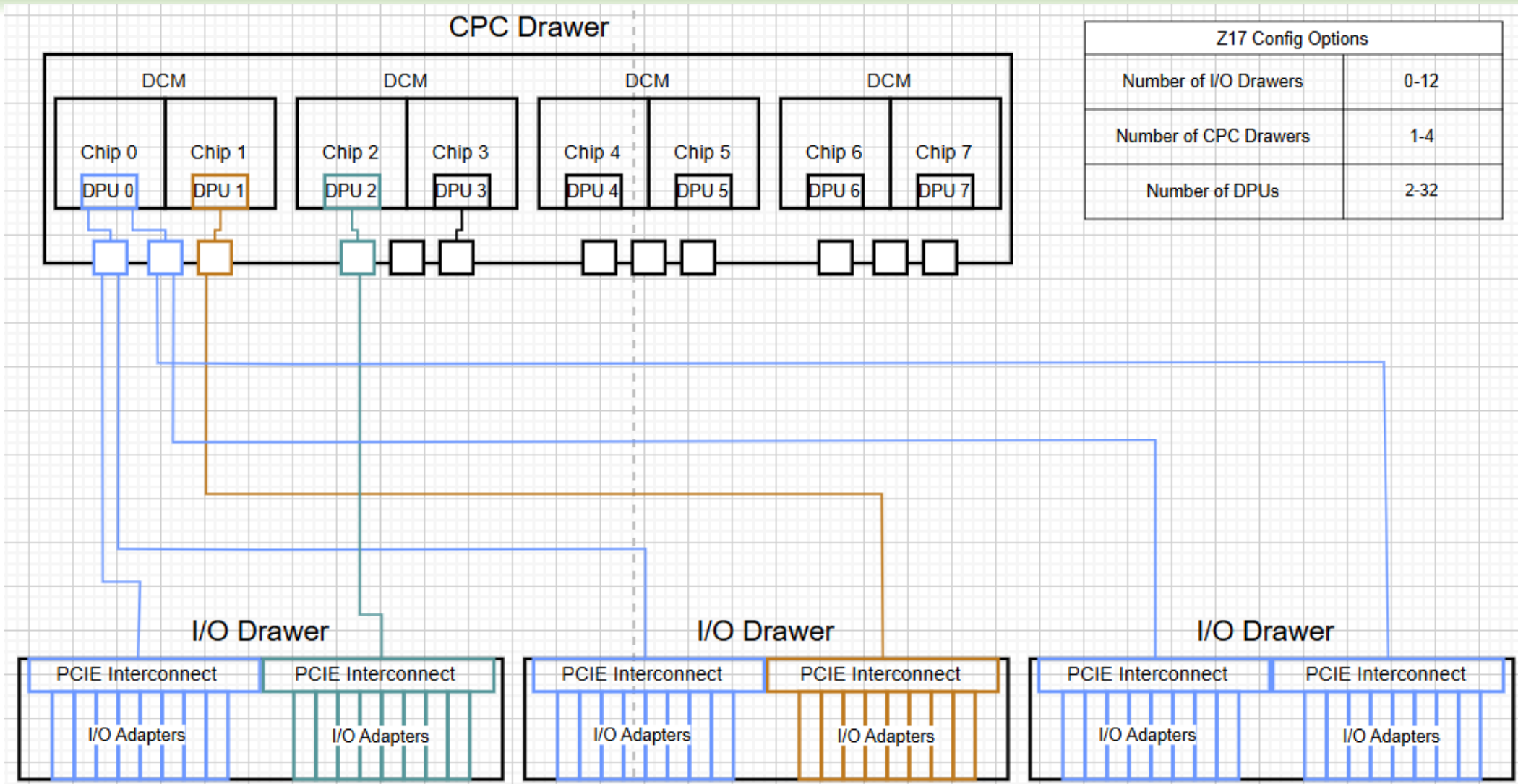
- DPUs do NOT share compute with each other
- Each channel is processed by a single DPU
- Each DPU can process up to 128 Channels
- DPU channel links determined by hardware configuration
- The ONLY adapters which use the DPU are the FICON Express 32-4p and the Network Express adapters

Time/ CHPID	Chnl Type	DPU Num	<DPU Util Pct-> <CHPID>	<-DPU->

06:02:00				
20	FCS	22	0.005	0.064
21	FCS	30	0.005	0.045
22	FCS	22	0.005	0.064
23	FCS	30	0.005	0.044
24	FCS	22	0.005	0.064
25	FCS	30	0.005	0.045
26	FCS	22	0.005	0.064
27	FCS	30	0.005	0.045
C8	FCP	14	0.003	0.058
CB	FCP	14	0.003	0.058
CD	FCP	22	0.003	0.064
E0	OSD	.	.	.
E1	OSD	.	.	.
E2	OSD	.	.	.
E3	OSD	.	.	.
E5	OSD	.	.	.
E7	OSD	.	.	.
E8	OSD	.	.	.
E9	OSD	.	.	.

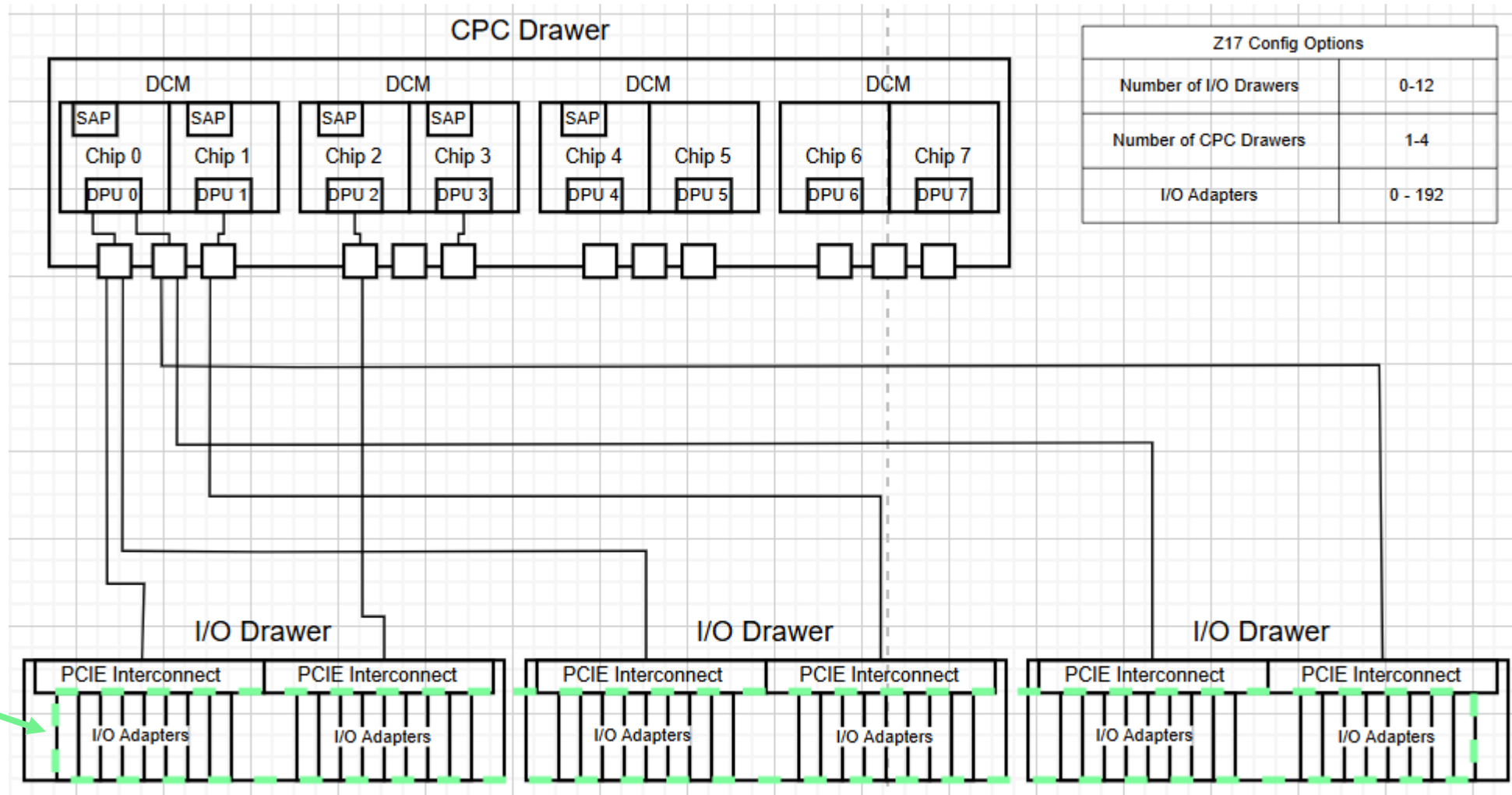
Totals	FICON	.	0.042	.
Totals	FCP	.	0.036	.
Totals	OSA	.	0	.

z17 Channel Components - DPU



Sample z17 I/O drawer Configuration

z17 Channel Components – I/O Adapter



I/O Adapters

Sample z17 I/O drawer Configuration

z17 Channel Components/Metrics – I/O Adapter

Description

- Facilitates data transfer between the mainframe box and outside networks/devices

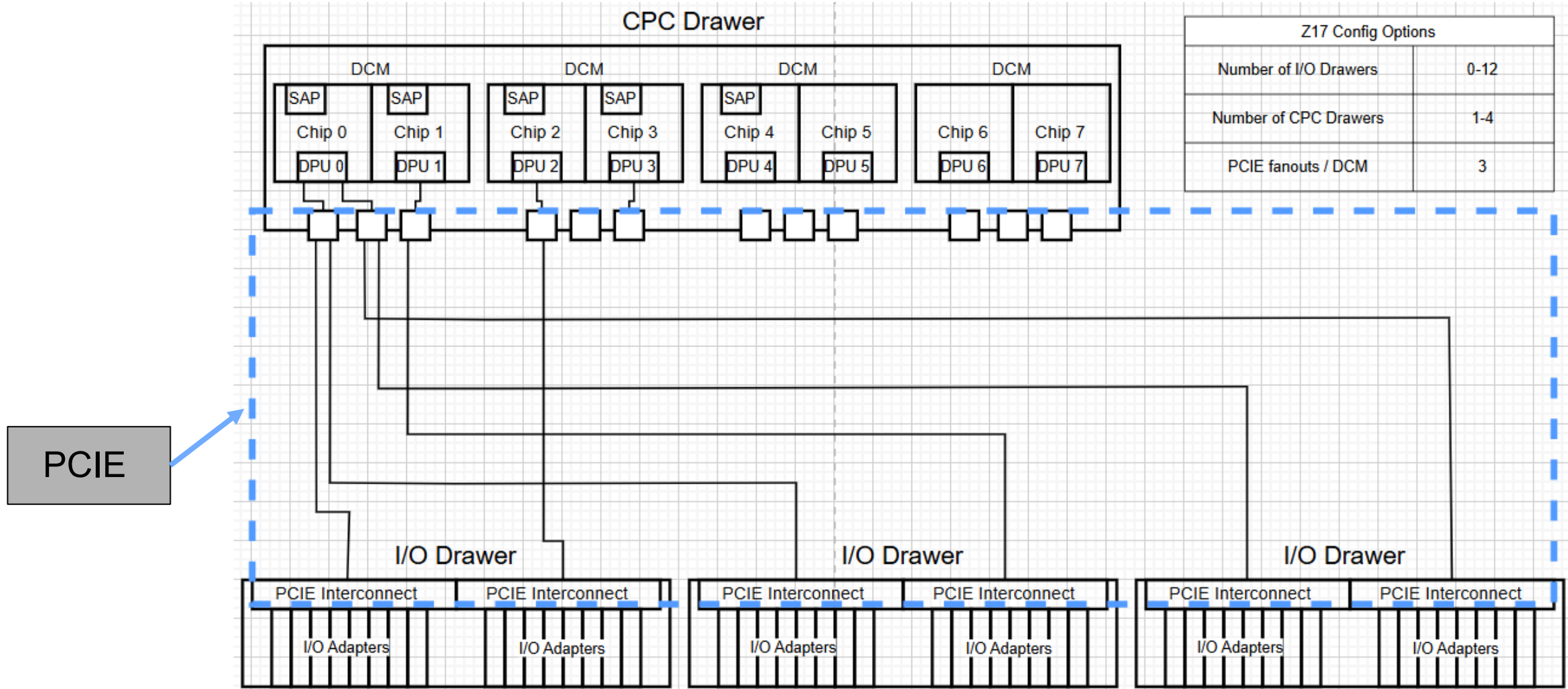
Relevant Performance Details

- Maximum utilization is based on I/O Adapter model
- Separate maximums for reads and writes

Time/ CHPID	Chnl Type	<-----Data Units----->			<-----Data Units----->		
		<Reads/Second-> LPAR	Total Pct	<Writes/Second-> LPAR	Total Pct	<Writes/Second-> LPAR	Total Pct
06:02:00							
20	FCS	11	2374 0.1	32	2208 0.1		
21	FCS	10	2377 0.1	14	2073 0.1		
22	FCS	13	2446 0.1	14	2043 0.1		
23	FCS	12	2426 0.1	20	2117 0.1		
24	FCS	12	2390 0.1	21	1982 0.1		
25	FCS	16	2338 0.1	27	2056 0.1		
26	FCS	11	2425 0.1	40	2231 0.1		
27	FCS	17	2309 0.1	22	1926 0.1		
C8	FCP	0	139 0.0	0	5411 0.2		
CA	FCP	0	47 0.0	0	5028 0.2		
CB	FCP	0	163 0.0	0	6446 0.2		
CD	FCP	0	149 0.0	0	6954 0.2		
E0	OSD	99	3153 0.5	931	2176 0.3		
E1	OSD	243	1898 0.3	0	3856 0.6		
E2	OSD	80	2100 0.3	482	4752 0.7		
E3	OSD	386	2420 0.4	262	3436 0.5		
E5	OSD	211	2483 0.4	97	6482 1.0		
E7	OSD	83	4224 0.7	272	1570 0.2		
E8	OSD	387	2390 0.4	83	1635 0.3		
E9	OSD	109	1820 0.3	122	2003 0.3		
Totals	FICON	101	19085 0.6	190	16634 0.5		
Totals	FCP	3918	5956 0.2	15948	75658 2.3		
Totals	OSA	1599	20487 3.2	2250	25910 4.0		

Report displaying, I/O Control Unit Read/Write Utilization by CHPID

z17 Channel Components



Sample z17 I/O drawer Configuration

z17 Channel Components - PCIE

Description

- Expansion bus connecting chips on the CPC drawer to devices on the I/O drawer

Relevant Performance Details

- PCIEs have 1 set of wires for sending data and 1 set of wires for receiving data

Time/ CHPID	Chnl Type	<Bus Cy> <c1/Sec> Used Pct	
-----	-----	-----	----
06:02:00			
20	FCS	4582	0.1
21	FCS	4450	0.1
22	FCS	4488	0.1
23	FCS	4543	0.1
24	FCS	4372	0.1
25	FCS	4394	0.1
26	FCS	4656	0.1
27	FCS	4235	0.1
C8	FCP	5360	0.1
CA	FCP	4020	0.1
CB	FCP	7763	0.2
CD	FCP	6700	0.2
E0	OSD	.	.
E1	OSD	.	.
E2	OSD	.	.
E3	OSD	.	.
E5	OSD	.	.
E7	OSD	.	.
E8	OSD	.	.
E9	OSD	.	.
-----	-----	-----	----
Totals	FICON	36K	0.6
Totals	FCP	38K	1.0
Totals	OSA	0	0

Report displaying PCIE bus cycle utilization by CHPID

So, what do you do when there is an I/O problem?

Thank you for listening!

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